WHAT IS CLAIMED IS:

1. A ferroelectric memory device comprising:

an interlayer dielectric layer;

a protection adhesion layer on the interlayer dielectric layer;

a buried contact extending through the protection adhesion layer and the interlayer dielectric layer;

a lower electrode on a portion of the protection adhesion layer adjacent to the buried contact and on the buried contact;

a ferroelectric layer covering the lower electrode and the protection adhesion layer; and

an upper electrode overlapping with the lower electrode and covering the ferroelectric layer.

2. A ferroelectric memory device according to Claim 1 wherein the buried contact comprises:

an upper buried contact portion comprising a barrier pattern extending from the lower electrode through the protection adhesion layer; and

a lower buried contact portion extending from the barrier pattern through the interlayer dielectric layer.

3. A ferroelectric memory device according to Claim 1 wherein the protection adhesion layer comprises titanium oxide layer (TiO_2).

4. A ferroelectric memory device according to Claim 2 wherein the barrier pattern is selected from the group consisting of TiN, TiAlN, $TiSi_x$, TiSiN, TaSiN and TaAlN.

5. A ferroelectric memory device according to Claim 1 wherein the ferroelectric layer is selected from the group consisting of PZT[Pb(Zr, Ti)O_3], $PbTiO_3$, $SrTiO_3$, $BaTiO_3$, $PbLaTiO_3$, (Pb, La) (Zr, Ti)O_3, BST[(Ba, Sr)TiO_3], $Ba_4Ti_3O_{12}$, $SrBi_2Ta_2O_9$ and $Bi_4Ti_3O_{12}$.

6. A ferroelectric memory device according to Claim 1 wherein the lower electrode and the upper electrode are selected from the group consisting of ruthenium (Ru), platinum (Pt), rhodium (Rh), osmium (Os), palladium (Pd), ruthenium oxide (RuO_x), iridium oxide (IrO_x) and platinum oxide (PtO_x), rhodium oxide (RhO_x), osmium oxide (OsO_x) and palladium oxide (PdO_x).

7. A ferroelectric memory device according to Claim 1 wherein the buried contact is selected from the group consisting of tungsten, aluminum, copper and polysilicon doped or undoped with impurities.

8. A ferroelectric memory device according to Claim 1 wherein the lower electrode comprises one of a plurality of lower electrodes, wherein the upper electrode overlaps at least two of the plurality of lower electrodes.

9. A ferroelectric memory device according to Claim 8 further comprising:

an upper interlayer dielectric layer covering the ferroelectric layer and the upper electrode; and

a plate line electrically connected to the upper electrode through the upper interlayer dielectric layer.

10. A ferroelectric memory device according to Claim 8 further comprising:

a strip line on the upper interlayer dielectric layer; and

an upper metal interlayer dielectric layer covering the strip line, wherein the plate line is electrically connected to the upper electrode through the upper metal interlayer dielectric layer and the upper interlayer dielectric layer.

11. A method of forming a ferroelectric memory device comprising:

forming an interlayer dielectric layer and a protection adhesion layer on a substrate respectively;

forming a contact hole through the interlayer dielectric layer and the protection adhesion layer to expose the substrate;

forming a buried contact in the contact hole that extends through the interlayer dielectric layer and the protection adhesion layer;

forming a lower electrode on the buried contact and on a portion of the protection adhesion layer adjacent to the buried contact to leave a remaining portion of the protection adhesion layer exposed;

forming a ferroelectric layer on the lower electrode and on the protection adhesion layer; and

forming an upper electrode on the ferroelectric layer and overlapping the lower electrode.

12. A method according to Claim 11 wherein forming a buried contact comprises:

forming an upper buried contact portion comprising a barrier pattern extending from the lower electrode through the protection adhesion layer; and

forming a lower buried contact portion extending from the barrier pattern through the interlayer dielectric layer.

13. A method according to Claim 11 wherein the protection adhesion layer comprises a titanium oxide layer.

14. A method according to Claim 11 wherein forming a buried contact comprises:

forming a conductive layer on an entire surface of the substrate including in the contact hole to fill the contact hole with the conductive layer; and

planarizing the conductive layer to expose the protection adhesion layer and to form the buried contact in the contact hole.

15. A method according to Claim 11, the method further comprising before forming the lower electrode:

recessing the buried contact to within the contact hole to form an upper portion of the buried contact beneath the protection adhesion layer;

forming a barrier layer in the contact hole on the upper portion of the buried contact to fill the contact hole; and

planarization the barrier layer to expose the protection adhesion layer and to form a barrier pattern on the upper portion of the buried contact.

16. A method according to Claim 15 wherein the barrier pattern comprises a material selected from the group consisting of TiN, TiAlN, $TiSi_x$, TiSiN, TaSiN and TaAlN.

17. A method according to Claim 15 wherein forming a barrier layer comprises forming the barrier layer using at least one method selected from the group consisting of sputtering, chemical vapor deposition, sol-gel and atomic layer deposition.

18. A method according to Claim 11 wherein the ferroelectric layer comprises a material selected from the group consisting of PZT[Pb(Zr, Ti)O_3], $PbTiO_3$, $SrTiO_3$, $BaTiO_3$, $PbLaTiO_3$, (Pb, La) (Zr, Ti)O_3, BST[(Ba, Sr)TiO_3], $Ba_4Ti_3O_{12}$, $SrBi_2Ta_2O_9$ and $Bi_4Ti_3O_{12}$.

19. A method according to Claim 11 wherein the lower electrode and the upper electrode are formed of a material selected from the group consisting of ruthenium (Ru), iridium (Ir), platinum (Pt), rhodium (Rh), osmium (Os), palladium (Pd), iridium oxide (IrO_x), and platinum oxide (PtO_x), rhodium oxide (RhO_x), osmium oxide (OsO_x) and palladium oxide (PdO_x).

20. A method according to Claim 11 wherein forming a lower electrode comprises forming a plurality of lower electrodes, wherein forming an upper electrode comprises forming the upper electrode overlapping at least two of the plurality of lower electrodes.

21. A method according to Claim 20 further comprising:

forming an upper interlayer dielectric layer covering the ferroelectric layer and the upper electrode; and

forming a plate line electrically connected to the upper electrode through the upper interlayer dielectric layer.

22. A method according to Claim 21 further comprising before forming the plate line:

forming a strip line on the upper interlayer dielectric layer; and

forming an upper metal interlayer dielectric layer covering the strip line, wherein the plate line is electrically connected to the upper electrode through the upper metal interlayer dielectric layer and the upper interlayer dielectric layer.

23. A method according to Claim 22 wherein the interlayer dielectric layer, the upper interlayer dielectric layer and the upper inter-metal dielectric layer are formed using a method selected from the group consisting of PECVD (Plasma-enhanced chemical vapor deposition), LPCVD (Low-pressure chemical vapor deposition), ALD (Atomic layer deposition) and SOG (Spin on glass).

24. A method according to Claim 11 wherein the ferroelectric layer is formed using method selected from the group consisting of sputtering, CVD, sol-gel and atomic layer deposition.

25. A method according to Claim 11 wherein the buried contact comprises a material selected from the group consisting of tungsten, aluminum, copper and polysilicon doped or undoped with impurities.